

Surface Detector Trigger Operating Guide

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1 Introduction

This document the operation of the Auger SDE level 1 trigger, with emphasis on the register structure and programming issues. It is a completely rewritten evolution of the “Surface Detector Trigger ASIC/PLD Operating Guide”. Obsolete information has been removed, and the document has been re-organized to make it more maintainable. Therefore, the title has been changed, and the revision history reset.

1.1 Revision History

- Revision 1.00; initial version (August, 2002).
- Revision 1.01; small updates (October, 2002)
- Revision 1.02; simplify ID register plus other small updates (December, 2002)
- Revisions 1.03, 1.04; expand ID register; add enable for `_BUSERR` (January, 2003)
- Revision 1.05; update scaler, muon memory, chip ID, and global control documentation (March 2003). Valid for code versions x170303y and later.
- Revision 1.06; add description of TC0 and TC1. Add control bit in GLOBAL CONTROL register. (March 2003). Valid for code versions x310303y and later.
- Revision 1.07; modify muon trigger so that 3 bins are saved prior to the triggering bin rather than just one; add option to invert normal sense of external trigger input from low true to high true; increase muon trigger A burst length to 20, muon trigger B burst length to 8 (April 2003). Valid for code versions x250403y and later.
- Revision 1.08; fix error in resetting muon buffer full condition when the buffer becomes full via running out of space (as opposed to via time-out); clarify muon word count and read sequence documentation (July 2003). Valid for code versions x070703y and later.
- Revision 1.09; add option to store low instead of high order ADCs in PLDb memory to facilitate testing those connections; fix small error in shower memory readout; modify External Trigger to be edge triggered; fix muon buffer Time Tag B; remove some redundant register readbacks to save PLD space; add pedestal tracking modules (October 2003). Valid for code versions x221003y and later.

- Revision 1.10; add option to pre-scale any trigger by 256; add readout of fractional computed pedestal; add latching of computed pedestal on shower trigger; remove unused muon trigger B and single bin sum triggers; reduce maximum width & occupancy of TOTb to 127; reduce maximum width & occupancy of TOTc to 63 (November 2003). Valid for code versions x241103y and later.
- Revision 1.11; add option to require 2 consecutive bins above threshold in single bin trigger; change muon buffer burst behavior to have fixed 20 bin length instead of retriggering; remove TC0, TC1 outputs and corresponding controls from GLOBAL CONTROL register; add ADC ERROR COUNT register (July 2004). Valid for code versions x290704y and later.
- Revision 1.12; replace the 2 scaler instances with 3 simpler scaler instances; add timing information table; make small transparent changes to improve timing margin for first word read via DMA (February 2005). Valid for code versions x030205y and later.
- Revision 1.13; update number of wait states needed during programming to work with prototype Cyclone boards. Change in documentation only, no change in PLD code. Valid for code versions x030205y and later.
- Revision 1.14; Improve tracking for ADC_FILTER. Fix documentation error regarding ADC_FILTER register. Valid for code versions x190705y and later.
- Revision 1.15; Add AMIGA trigger. Add “time-over-threshold-deconvoluted” (ToTd) trigger. Remove instances B and C of ToT trigger. Remove ADC filter. **Note that there are changes to the TRIGGER_MASK and TRIGGER_ID registers.** Valid for code versions x040410y and later.
- Revision 1.16; Increase ToTd maximum window width from 63 to 127; fix PMT enable logic for ToTd trigger; remove input signal routing to allow ToTd changes. Valid for code versions x270211y and later.
- Revision 1.17; Decrease ToTa maximum window width from 255 to 127; add MoPS trigger. Valid for code versions x270711y and later.
- Revision 1.18; Add TRIG_RATES module to count the rates of the various level 1 triggers. Valid for code versions x280911y and later.
- Revision 1.19; Add integral signal requirement to MoPS trigger; remove variable window width feature from ToT and ToTd triggers (now fixed at 120 bins). Valid for code versions x121211y and later.
- Revision 1.20; Add integral signal requirement to ToTd trigger; tweak input to EVTCLKF delay; moved trigger delays table to separate document; removed trigger interface section. Valid for code versions x161012y and later.
- Revision 1.21; Modify details of integral signal integration so that the integral remains valid for delayed triggers; changed MoPS window to 120 bins, the same as ToT and ToTd. Valid for code versions x070113y and later.

2 Overview

The trigger circuitry is partitioned among 3 chips; 2 Altera PLDs and one IDT static RAM (Cyclone versions of the front-end board have one PLD and one static RAM). These chips interface with 6 Analog Devices ADCs which digitize tank PMT signals. They also interface with the station controller PowerPC (PPC403GCX) processor.

3 Register Usage

The register address space of the trigger circuitry occupies 128 registers. The register definitions have been structured to incorporate the best features of the precursor PLD and ASIC designs. However, the addresses of the registers in the precursor designs is not consistent with the partitioning of the current design into 2 PLDs. Therefore, the opportunity was taken to better organize the register address structure into functional groups. Each of these is described below.

3.1 ADC filter

The input ADC signals may be processed through a digital filter to stabilize the pedestal. The filter implements a Σ, δ measurement of the pedestal, comparing the measured pedestal with the ADC value in each time bin. If the signal is greater than the measured pedestal, the measured pedestal is incremented by δ . If it is less it is decremented by δ . The value of δ is set to 1/256 count, so that the maximum rate of change of the measured pedestal is 1 count per 6.4 μs . This method decouples the pedestal determination from the influence of large signals, since only the sign, and not the magnitude of signal deviations from the measured pedestal is utilized. The measured pedestal is subtracted from the data, and the target pedestal is added. This filter is controlled by the following set of registers.

Name	Address	Width	Description
ADC[9:0] FILTER	base+0	30	Pedestal & enable for ADC[9:0]
ADC[19:10] FILTER	base+1	30	Pedestal & enable for ADC[19:10]
ADC[29:20] FILTER	base+2	30	Pedestal & enable for ADC[29:20]
ADC[39:30] FILTER	base+3	30	Pedestal & enable for ADC[39:30]
ADC[49:40] FILTER	base+4	30	Pedestal & enable for ADC[49:40]
ADC[59:50] FILTER	base+5	30	Pedestal & enable for ADC[59:50]

Please note that registers at addresses base+0 through base+2 above read back at both their base addresses and their shadow addresses, as the information is utilized in both PLDa and PLDb. Registers at addresses base+3 through base+5 are written at the base addresses, but can only be read back at their shadow addresses.

Bit usage for each of the ADC FILTER registers is as follows:

Bit(s)	Description
9:0	Target value for pedestal of filtered ADC data.
10	Enable filter if set.
11	Not used
19:12	Fractional portion of current pedestal value determined by the filter module.
29:20	Integer portion of current pedestal value determined by the filter module.

Note: Previously implemented ADC filter is not present in code versions x040410y and later.

3.2 Input signal

Input signal routing is managed by the following set of registers. This routing occurs after any input filtering. Thus internally generated test patterns are not filtered.

Name	Address	Width	Description
CONTROL	base+0	7	Control register for data source
MODE	base+1	12	Specifies test pattern mode
ADC[9:0] TEST	base+2	10	Initial test pattern for ADC[9:0]
ADC[19:10] TEST	base+3	10	Initial test pattern for ADC[19:10]
ADC[29:20] TEST	base+4	10	Initial test pattern for ADC[29:20]
ADC[39:30] TEST	base+5	10	Initial test pattern for ADC[39:30]
ADC[49:40] TEST	base+6	10	Initial test pattern for ADC[49:40]
ADC[59:50] TEST	base+7	10	Initial test pattern for ADC[59:50]

Please note that registers at addresses base+0 through base+4 above read back at both their base addresses and their shadow addresses, as the information is utilized in both PLDa and PLDb. Registers at addresses base+5 through base+7 are written at the base addresses, but can only be read back at their shadow addresses.

Bit usage for the CONTROL register is as follows:

Bit(s)	Description
5:0	Enable bit for each of 6 ADC inputs: 0=use ADC, 1=use test pattern.
6	Route low order instead of high order ADCs to PLDb memory if set.

The test pattern generates a either a fixed value, a sawtooth, or rotating bit waveform for each ADC input channel. The sawtooth is useful for verifying the design in simulation. The rotating bit pattern gives better coverage for testing. The MODE register specifies the form of the test pattern. Bit usage for the MODE register is as follows:

Bit(s)	Description
5:0	Specifies fixed or variable pattern for each ADC input: 0=fixed, 1=variable.
11:6	If variable, specifies whether the pattern counts up or rotates: 0=count, 1=rotate.

Note: Previously implemented ADC input signal routing is not present in code versions x270211y and later.

3.3 Single bin trigger

Single bin triggers operate on a single ADC time bin. This trigger is controlled by the registers shown below.

Name	Address	R/W	Width	Description
THR0	base+0	R/W	10	Threshold for PMT1
THR1	base+1	R/W	10	Threshold for PMT2
THR2	base+2	R/W	10	Threshold for PMT3
THRSUM	base+3	R/W	12	No longer used
ENABLE	base+4	R/W	10	Control bits for the trigger

The bit usage for the ENABLE register is as follows:

Bit(s)	Description
0	No longer used
1	No longer used
2	No longer used
3	Include PMT1 in multiplicity logic if set
4	Include PMT2 in multiplicity logic if set
5	Include PMT3 in multiplicity logic if set
7:6	Coincidence level for multiplicity logic sub-trigger
8	No longer used
9	Require 2 consecutive bins above threshold if set

3.4 Time-over-threshold trigger

The time-over-threshold trigger first applies trigger conditions of the type used for the single bin trigger to individual bins, then counts the number of bins within a sliding window which meet those conditions. If the occupancy exceeds a specified value, a time-over-threshold shower trigger is generated.

A block of 7 registers controls each time-over-threshold trigger instance.

Name	Address	R/W	Width	Description
THR0	base+0	R/W	10	Threshold for PMT1
THR1	base+1	R/W	10	Threshold for PMT2
THR2	base+2	R/W	10	Threshold for PMT3
THRSUM	base+3	R/W	12	No longer used
ENABLE	base+4	R/W	10	Control bits for the trigger
WID	base+5	R/W	7	Width in bins of sliding window (see below!)
OCC	base+6	R/W	7	Occupancy required for trigger

The bit usage for the ENABLE register is the same as for the single bin trigger above.

The sub-trigger that feeds the time-over-threshold occupancy logic is the logical OR of the enabled multiplicity and pulse height sum sub-triggers.

Note: Previously implemented trigger instances B and C are not present in code versions x260210y and later.

Note: The maximum WID and OCC is reduced to 127 starting with code versions x270711y.

Note: WID is fixed at 120 bins starting with code versions x121211y.

3.5 Time-over-threshold trigger (deconvoluted)

The time-over-threshold-deconvoluted trigger first deconvolutes the typical exponential fall from the FADC trace, secondly applies a pulse height window to each deconvoluted trace, and thirdly counts the number of bins within a sliding window which meet pulse height window conditions. Finally, if the occupancy exceeds a specified value in the required multiplicity of deconvoluted traces, a time-over-threshold-deconvoluted shower trigger is generated. Please note that the order of operations is not the same as for the time-over-threshold trigger above.

Also note that as of version x161012y the signal integral condition in the MOPS trigger registers is also applied to the ToTd trigger, and that the same threshold for the integral applies.

A block of 11 registers controls the time-over-threshold-deconvoluted trigger instance.

Name	Address	R/W	Width	Description
THR0	base+0	R/W	10	Lower threshold for PMT1
THR1	base+1	R/W	10	Lower threshold for PMT2
THR2	base+2	R/W	10	Lower threshold for PMT3
UP0	base+3	R/W	10	Upper threshold for PMT1
UP1	base+4	R/W	10	Upper threshold for PMT2
UP2	base+5	R/W	10	Upper threshold for PMT3
ENABLE	base+6	R/W	8	Control bits for the trigger
WID	base+7	R/W	7	Width in bins of sliding window (see below!)
OCC	base+8	R/W	7	Occupancy required for trigger
FD	base+9	R/W	6	Decay constant - binary fraction
FN	base+a	R/W	6	Normalizer - binary fixed point

Note that the THR_x and OCC conditions are satisfied when the signal is strictly greater than (>) the register value, while UP_x condition is satisfied when the signal is less than or equal to (≤) the register value. Thus writing 1023 to an UP_x register disables that constraint.

The bit usage for the ENABLE register is shown below.

Bit(s)	Description
0	Not used
1	Not used
2	Not used
3	Include PMT1 in multiplicity logic if set
4	Include PMT2 in multiplicity logic if set
5	Include PMT3 in multiplicity logic if set
7:6	Coincidence level for multiplicity logic sub-trigger

FD is obtained from $FD = e^{-\Delta t/\tau}$ where $\Delta t = 25ns$, and τ is the decay time of light in the tank. FD is 6 binary digits constrained to be less than 0.75. The value of FN to load is determined by FD from the equation $FN = 1/(1 - FD)$. It is loaded as a fixed point number xx.yyyy, and must be less than 4. Values of FD and FN are within the allowed range for $\tau \leq 80$ ns.

The following logic can be used to obtain the values of FD and FN to load in the registers.

$$FD = (int)(64. * e^{-\Delta t/\tau} + 0.5)$$

$$FN = (int)(1024./(64. - FD) + 0.5)$$

This trigger is present in code versions x040410y and later.

Note: WID is fixed at 120 bins starting with code versions x121211y.

3.6 Multiplicity of Positive Steps

The multiplicity-of-positive-steps (MOPS) trigger counts positive steps in each FADC trace, accumulating bin to bin steps until the first bin which is smaller than the previous bin is encountered. The aggregate positive step is then

subjected to a minimum & maximum height constraint. If it passes this condition the step is added to the count of such steps within a fixed length 120 bin long sliding window. A variable length veto may be applied to ignore aggregate steps following another such step. Finally, if the occupancy exceeds a specified value in the required multiplicity of traces, and the integrated signal exceeds a specified value in those same traces, a multiplicity-of-positive-steps trigger is formed.

The signal integration operates by keeping a running sum of the pulse height in the current ADC time bin minus that in the bin 250 time slots earlier. However, there is a period after a trigger, when no triggers are possible due to finishing the ADC trace or if no buffers are available, in which the earlier time bin is not available in the PLD. While this does not affect any triggered events, it could cause the integrated signal to diverge from zero. In order to mitigate this effect, the integrated signal is exponentially decayed with a time constant of 2048 time bins. The actual integral decays faster than that due to the undershoot following a signal. Note that in any case, the integral depends upon the history of signals not only in the trace, but before the trace, so an exact offline reconstruction of the trigger is not possible. The integral remains valid for ≈ 250 time bins after the primary trigger.

A block of 10 registers controls the multiplicity-of-positive-steps trigger instance.

Name	Address	R/W	Width	Description
MIN0	base+0	R/W	10	Lower threshold for PMT1
MIN1	base+1	R/W	10	Lower threshold for PMT2
MIN2	base+2	R/W	10	Lower threshold for PMT3
MAX0	base+3	R/W	10	Upper threshold for PMT1
MAX1	base+4	R/W	10	Upper threshold for PMT2
MAX2	base+5	R/W	10	Upper threshold for PMT3
ENABLE	base+6	R/W	8	Control bits for the trigger
INT	base+7	R/W	10	Minimum integrated signal
OCC	base+8	R/W	7	Occupancy required for trigger
OFS	base+9	R/W	4	Veto

Note that the MIN_x, OCC, and INT conditions are satisfied when the signal is strictly greater than ($>$) the register value, while MAX_x condition is satisfied when the signal is less than or equal to ($\leq$) the register value. Thus writing 1023 to a MAX_x register disables that constraint.

The veto is active for $\max(0, \text{int}(\log_2(ph)) + 1 - ofs)$ bins following a aggregate step of size ph . The veto can be disabled by setting OFS to 10 (decimal). Also note that a veto length of 1 has no effect since at least on negative bin to bin step is required to finish an aggregate step. The following table lists some example veto durations.

OFS	Aggregate step	Veto duration
0	2	2
0	3	2
0	9	4
1	2	1
1	5	2
1	8	3
2	8	2
4	8	0

The bit usage for the ENABLE register is shown below.

Bit(s)	Description
0	Not used
1	Not used
2	Not used
3	Include PMT1 in multiplicity logic if set
4	Include PMT2 in multiplicity logic if set
5	Include PMT3 in multiplicity logic if set
7:6	Coincidence level for multiplicity logic sub-trigger

This trigger is present in code versions x270711y and later. The minimum integrated signal requirement is present in code versions x081211y and later. Note this uses the register previously used to specify the window length.

Also note that as of version x161012y the minimum integrated signal requirement set for the MOPS trigger is also applied to the ToTd trigger.

3.7 Random Trigger

The random trigger provides a means for the PPC403 to generate a trigger after a specified delay, irrespective of the ADC inputs. It is controlled by a bank of 3 registers.

Name	Address	R/W	Width	Description
DELAY A	base+0	R/W	12	Low order 12 bits of delay (25ns increments)
DELAY B	base+1	R/W	12	High order 12 bits of delay (25ns increments)
START	base+2	W	–	Writing anything to this register starts the random trigger timer

Only 1 random trigger is generated per write to the START register. Also note that the trigger inhibit will block random triggers with less than 256 clock cycle delay.

3.8 Shower memory

This bank of registers controls aspects of the shower memories and provides status information.

Name	Address	R/W	Width	Description
TRIGGER MASK	base+0	R/W	15	Mask of allowed triggers
TRIGGER ID	base+1	R	15	Indicates the trigger for the buffer being read
CONTROL	base+2	R/W	4	Controls the DMA readout sequence
STATUS	base+3	R	26	Reports shower memory buffer status

The following bits are defined in the TRIGGER MASK register. Note that the external trigger is enabled by default after a reset. **Note that some of the mask bits have changed starting in code version x040410y. Note further changes starting in code version x072711y.**

Bit(s)	Description
0	Single bin trigger
1	Time-over-threshold A trigger
2	Time-over-threshold deconvoluted trigger
3	Multiplicity-of-positive-steps trigger
4	External trigger
5	Random trigger
6	Pre-scale single bin trigger by 256 if set
7	Pre-scale time-over-threshold A trigger if set
8	Pre-scale time-over-threshold deconvoluted trigger if set
9	Pre-scale MoPS trigger if set
10	Pre-scale external trigger if set
11	Pre-scale random trigger if set

The following bits are defined in the TRIGGER ID register. The initial trigger bits indicate which trigger generated the T1 trigger from the logic. The additional trigger bits flag any trigger conditions that are satisfied by the FADC traces after an initial trigger. **Note that some of the ID bits have changed starting in code version x040410y. Note further changes starting in code version x072711y.**

Bit(s)	Description
0	Initial single bin trigger
1	Initial time-over-threshold A trigger
2	Initial time-over-threshold deconvoluted trigger
3	Multiplicity-of-positive-steps trigger
4	Initial external trigger
5	Initial random trigger
6-7	Not used
8	Additional single bin trigger
9	Additional time-over-threshold A trigger
10	Additional time-over-threshold deconvoluted trigger
11	Additional multiplicity-of-positive-steps trigger
12	Additional external trigger
13	Additional random trigger

The following bits are defined in the CONTROL register.

Bit(s)	Description
0	Reset buffer pointers to prepare buffer for read (or re-read)
1	Prefetch data from memory to fill readout pipeline. Reads back as 0.
2	Selects whether PLDa or PLDb provides the data during DMA. 0: Subsequent DMA is low order ADC data from PLDa. 1: Subsequent DMA is high order ADC data from PLDb.
3	Reset buffer full status; reset write pointers; release buffer to accept new data. Reads back as 0.

The following bits are defined in the STATUS register.

Bit(s)	Description
2:0	EVTSYNF for the current buffer to be read
5:3	EVTSYNF for buffer 0
8:6	EVTSYNF for buffer 1
9	Buffer number that will be/was read
10	Full flag for buffer 0
11	Full flag for buffer 1
15:12	Not used
25:16	Number of words read from buffer

3.9 Trigger Rates

The trigger rates block counts reports the rates of several of the triggers accumulated over the last 26.8 seconds. The rate counters are double buffered, so there is always a static value representing the number of triggers during a 26.8 second interval that ended some time between 0 and 26.8 seconds ago. The trigger rate registers are organized as follows:

Name	Address	R/W	Width	Description
TRIGGER RATES	base+0	R	32	Rates for single bin, ToT, ToTd, and MoPS triggers
DELAYED RATES	base+1	R	32	Rates for single bin, ToT, ToTd, and MoPS delayed triggers

The information is packed in each of these two registers as follows:

Bit(s)	Description
7:0	# single bin triggers in last 26.8 seconds / 32
15:8	# ToT triggers in last 26.8 seconds
23:16	# ToTd triggers in last 26.8 seconds
31:24	# MoPS triggers in last 26.8 seconds

The counts in each field are limited to a maximum value of 252 (fc_{16}). Any rate higher than 252 per 26.8 second interval will read as 252. For example, any ToTd rate higher than about 9.38 Hz will read 252.

3.10 Muon triggers

The muon trigger registers are organized as follows:

NAME	Address	R/W	Width	Description
MU TRIGGER	base-base+4	R/W	Varies	Muon trigger registers

The MU TRIGGER blocks has the same format as the single bin trigger block described above.

3.11 Muon memory buffers

This bank of registers controls aspects of the muon memory buffers and provides status information. The first buffer is not active until the TRIGGER MASK register is written. Subsequent writes to the TRIGGER MASK register will restart the current buffer from the beginning.

Name	Address	R/W	Width	Description
BUF TIMER A	base+0	R/W	12	Low order 12 bits of muon buffer timer (25ns increments)
BUF TIMER B	base+1	R/W	12	High order 12 bits of muon buffer time
TIME TAG A	base+2	R	30	Time tag at the beginning of the buffer
TIME TAG B	base+3	R	30	Time tag at the end of the buffer
TRIGGER MASK	base+4	R/W	3	Mask of allowed triggers
CONTROL	base+5	W	5	Controls the DMA readout sequence
STATUS	base+6	R	6	Reports muon memory buffer status
WORD COUNT	base+7	R	32	Reports number of words in memory & number read

The following bits are defined in the TRIGGER MASK register.

Bit	Description
0	Enable muon trigger if set
1	No longer used
2	Enable muon buffer timeout if set

The following bits are defined in the CONTROL register.

Bit(s)	Description
0	Reset buffer pointers to prepare buffer for read (or re-read)
1	Prefetch data from memory to fill readout pipeline. Reads back as 0.
2	Not used
3	Reset buffer full status; reset write pointers; release buffer to accept new data. Reads back as 0.
4	Force buffer full status for the buffer currently being written.

The following bits are defined in the STATUS register.

Bit(s)	Description
0	EVTSYNS for the current buffer to be read
1	EVTSYNS for buffer 0
2	EVTSYNS for buffer 1
3	Buffer number that will be/was read
4	Full flag for buffer 0
5	Full flag for buffer 1

The following bits are defined in the WORD COUNT register. The number of words available to be read from the memory is the write address minus 1.

Bit(s)	Description
13:0	Write address (14 low order bits)
15:14	Not used
29:16	Number of words read from buffer
31:30	Not used

3.12 Scalers

There are 3 32-bit scaler instances. Each scaler instance accumulates counts of a single bin trigger instance. The count can be reset by writing (anything) to the scaler register. Unlike code versions prior to x010105y, these scalers are no longer tied to muon buffer intervals and they are not double buffered. Scaler incrementing is inhibited while scaler is being read. Each scaler block has the following format.

Name	Address	R/W	Width	Description
Trigger Block	base+0:base+4	R/W	Varies	Block defining dedicated trigger
SOURCE MASK	base+5	R/W	7	Mask of sources for this scaler instance - no longer used
HOLDOFF	base+6	R/W	10	Minimum number of bins between triggers - no longer used
SCALER	base+7	R/W	32	Scaler value

The trigger block has the same format as the single bin trigger block described above. The scalers count on the leading edge of a trigger satisfied condition. After counting, the scalers will not count again until after the input data has fallen below the trigger threshold.

3.13 AMIGA trigger

This trigger block produces the interface signals for the AMIGA trigger. Only one register is used.

Name	Address	R/W	Width	Description
AMIGA GPS STAMP	15	W	24	GPS timestamp at trigger

3.14 Other

The following registers don't fit into any of the groupings above.

Name	Address	R/W	Width	Description
CHIP ID A	2f	R	32	ID register PLDa
CHIP ID B	7f	R	32	ID register PLDb
GLOBAL CONTROL	2e	W	2	Some global control operations
ADC ERROR COUNT	78	R	32	Counts ADC register errors

The ID registers contain the following bits.

Bits	Description
31:0	8 Hex digits: "Addmmyyn" for PLDa, "Bddmmyyn" for PLDb, where: "ddmmyy" represents the day/month/year of the code version release "n" is set to "0" for production code, and "d" for test versions.

The GLOBAL CONTROL register contains the following bits.

Bit(s)	Description
0	Generate a circuit wide reset (same as _RESET input signal)
1	Not used
2	Re-enable _RESET pin
3	No longer used
4	Invert normal sense of external trigger input from low active to high active

Writing a 1 to the GLOBAL CONTROL register will both generate a circuit wide reset and disable the _RESET pin. This is done because early versions of the UB code hold the _RESET pin low, preventing any useful operation of the trigger. The _RESET pin may be re-enabled after doing the above operation by writing a 4 to the GLOBAL CONTROL register.

The ADC ERROR COUNT register counts the number of clock cycles for which the low order bit of each high gain PMT registered in PLDa differs from the corresponding value registered in PLDb. The count is cumulative since the last global reset. This is mainly used as a diagnostic tool.

Note: _BUSERR output is not implemented in the current version of the code, irrespective of the setting of the bit in the global control register.

3.15 Address Map

The address structure is shown in the following table.

Address	Description
0-7	Input signal block
8-d	Input filter block
e-f	Reserved
10-14	Muon trigger block
15	AMIGA trigger
16-1f	Multiplicity-of-positive-steps trigger
20-27	Muon memory block
28-2b	Shower memory block
2c-2d	Trigger rates block
2e	GLOBAL CONTROL register
2f	ID register A
30-34	Single bin trigger block
35-37	Random trigger block
38-3e	Time-over-threshold trigger A block
3f	Reserved
40-4a	Time-over-threshold-deconvoluted trigger block
4b-4f	Reserved
50-57	Scaler A block
58-5f	Scaler B block
60-67	Scaler C block
68-6d	Shadow input filter register block
6e-6f	Reserved
70-77	Shadow input signal register block
78	ADC ERROR COUNT register
79-7a	Reserved
7b-7e	Shadow shower memory registers
7f	ID register B

4 PPC modes

4.1 Bank registers

There are 3 PPC403 bank registers that need to be configured for operation with the trigger circuitry.

4.1.1 PDT operations

Bank register 4 must be configured for PDT operations between the PPC403 and the trigger circuitry. Bank register 4 should be set to 20590583_{16} . This corresponds to CSON=1, HOLD=1, and 5 wait states.

4.1.2 PLD configuration

Bank register 6 must be configured for loading the configuration files into the PLDs. Bank register 6 should be set to 60190583_{16} . This corresponds to CSON=1, HOLD=1, and 5 wait states. This will work with both ACEX and Cyclone based boards.

4.1.3 DMA transfers

Bank register 7 must be configured for DMA transfers from the trigger circuitry into station controller memory. Bank register 7 should be set to 00b90ab0₁₆. This corresponds to “Burst Access=1” and “First Access=1”.

5 Shower Triggers & Memory

5.1 Register write order

To avoid spurious triggers, normally all registers should be loaded with their desired values before enabling any triggers in the Shower Memory TRIGGER MASK register. During test operations it may be desired to change the Input Signal ADC[xx:yy] registers while triggers are enabled. This is allowed, but be aware that changes are applied immediately upon the next rising CLK edge after the registers are written.

5.2 Shower memory writing

The storage of shower memory data is split between PLDa and PLDb. The format the data words is shown below.

Bits	Description
9:0	PMT1 ADC (low or high gain)
19:10	PMT2 ADC
29:20	PMT3 ADC
30	0 = High gain PMT channels, 1 = Low gain PMT channels
31	0

5.3 Reading shower memory

The shower memory can only be read after a trigger. The PPC403 is notified of a trigger by an active signal on _EVTCLKF.

The shower memory can currently be read only by DMA reads. Address bits are ignored for DMA reads. If more than one buffer is full, the oldest buffer is presented first. The shower memory is partitioned between PLDa and PLDb. PLDa contains the 3 high gain PMT inputs, PLDb contains the 3 low gain inputs. Up to 768 words may be read from each PLD. Shorter reads are allowed, but the same number of reads should be done to each PLD. If more than 768 words are read, data will still be presented to the bus, but the data words beyond the 768th from each PLD will be invalid. Note that this structure, which is utilized because of the relatively slow enable/disable of tri-state outputs in the PLDs, is different than that previously used.

It is not feasible to directly fetch data from the shower memory and place it on the data bus quickly enough to satisfy the timing constraints of the first word transferred during a DMA. The timing of subsequent transfers can be adjusted by setting “First Access” (which adds a delay before the 2nd word, but unfortunately not before the 1st data word is strobed into memory) and “Burst Access” (which adds delays for subsequent words) bits in the bank register. Therefore, one must pre-fetch the data (which also fills the memory read pipeline).

1. Write “1” to Shower Memory CONTROL register to prepare buffer for DMA read and select PLDa.
2. Write “2” to Shower Memory CONTROL register to pre-fetch the first word to output buffer.

3. Do DMA transfer of N words where $N \leq 768$ to get low order (high gain) ADC information.
4. Write “4” to Shower Memory CONTROL register to select PLDb.
5. Do DMA transfer of N words, where $N \leq 768$ to get high order (low gain) ADC information.
6. Read Shower Memory STATUS register to verify number of reads & obtain other status information.
7. Read Shower Memory TRIGGER ID register to find out what triggered the buffer just read.
8. Write “8” to Shower Memory CONTROL register to reset buffer full flags and make buffer ready to accept a new event.

5.4 External Trigger

Note that the external trigger comes up enabled after a general reset of the trigger circuitry. This is a provision for testing purposes in that it allows a 1-bit input signal `_EXTRG`, to result in a 1-bit output signal `_EVTCLKF`, without having to do any setup of the registers. An increment to the 3-bit `EVTSYNF` signal would also occur.

5.5 Random Trigger

A random trigger (or any other trigger for that matter) will be suppressed if it occurs within 768 clock cycles of a general reset of the trigger circuitry, a previous shower, external, or random trigger. A random trigger is suppressed for 256 clock cycles after a write to any register that could modify the trigger conditions (including starting a random trigger). A random trigger will also be suppressed if both memory buffers are full. The random trigger will not subsequently occur after any of the 768 clock cycle periods or after a memory buffer becomes available to record data unless the random trigger is again enabled by writing to the Random Trigger START register. That is, if a random trigger is blocked by one of the normal inhibit conditions (applied to any trigger), the random trigger behaves like other triggers and will not occur.

6 Muon Triggers & Memory

6.1 Register write order

To avoid spurious triggers, normally all registers should be loaded with their desired values before enabling any triggers in the Muon Memory TRIGGER MASK register. During test operations it may be desired to change the Input Signal registers while triggers are enabled. This is allowed, but be aware that changes are applied immediately upon the next rising CLK edge after the registers are written.

6.2 Muon memory writing

In contrast to the shower memory buffers, muon triggers do not cause CPU interrupts, they merely enable a short subsequent burst of data to be written to a muon memory buffer. A muon memory buffer is considered full, and an interrupt (`_EVTCLKS`) signal is sent to the PPC when either there is no more space in the memory buffer, or the muon memory BUF TIMER has expired, whichever occurs first.

When a MU TRIGGER condition is satisfied, a 30 bit time stamp is saved in memory. In addition the 3 high gain PMT channels for that time bin, the preceding 3 time bins, and the subsequent 16 bins are saved in the muon memory.

The muon buffers are stored in an external memory (IDT70V3569S - 16k*36bit Dual-Port static RAM). Two types of data are stored: ADC values, and time stamps. The format the ADC data words is shown below.

Bits	Description
9:0	PMT1 high gain ADC
19:10	PMT2 high gain ADC
29:20	PMT3 high gain ADC
30	Not relevant
31	0 – Indicates data word

The format of the time stamp data words is as follows.

Bits	Description
29:0	Time stamp
30	Not relevant
31	1 – Indicates time stamp

6.3 Reading muon memory

The muon memory can only be read after an _EVTCLKS interrupt to the PPC403 trigger. Muon Memory WORD COUNT register should be read before attempting to read the muon memory buffer. This operation returns the current write address pointer, N for the memory buffer. The number of words of data in the memory is $N - 1$. and will be between 0 and 8191. When reading the memory, the number of reads should be $< N$. Reads beyond $N - 1$ will return invalid data.

The procedure for reading out muon memory is:

1. Write 1 to the Muon Memory CONTROL register to reset buffer read pointer and number of words read portion of the Muon Memory WORD COUNT register.
2. Read Muon Memory WORD COUNT register and calculate number of words to transfer.
3. Read MU TIME TAG 1 register
4. Read MU TIME TAG 2 register. This corresponds (up to a fixed offset) to the time that the buffer was closed and _EVTCLKS was asserted. The difference indicated the time interval during which the muon buffer was active.
5. Write 2 to the Muon Memory CONTROL register to prefetch data from memory to fill the readout pipeline. This also removes the external IDT memory chip right port from “power down” mode.
6. Start DMA transfer
7. Wait for DMA transfer to finish
8. Read muon memory STATUS register to retrieve buffer status information.

9. Read muon memory WORD COUNT register to verify number of words transferred.
10. Write 8 to muon memory CONTROL register to prepare buffer to accept new data. This resets the initial write address and the full indicator. This also restores the external IDT memory chip right port to “power down” mode.

7 Timings

The delay between a signal at the input connector to the frontend board and the input to the PLD is $1.21\,\mu s$. For other delays please refer to the document “Trigger_delays.pdf”.